



Express Mail EV 493 481 970 US

Docket No.: T0461.70040 US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Stefan Marinca
Serial No.: 10/613,177
Confirmation No.: 6560
Filing Date: July 3, 2003
Title: CMOS BANDGAP CURRENT AND VOLTAGE GENERATOR

Examiner: R.B. Patel
Art Unit: 2838

Box Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith are the following documents:

- ☒ Issue Fee Transmittal
- ☒ Comments on statement of reasons for allowance
- ☒ Amendment after allowance
- ☒ Request for approval and entry of formal drawings (5 replacement sheets, Figs. 1-6)
- ☒ Return Receipt Postcard

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned at (617) 646-8000, Boston, Massachusetts.

A check is enclosed in the amount of \$1,700 to cover the filing fee. If the fee is insufficient, the balance may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

Respectfully submitted,

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Docket No.: T0461.70040 US00
Date: July 15, 2005

x07/22/05



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Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:


COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Applicant thanks the Examiner for the Statement of Reasons for Allowance. However, there are inaccuracies in the statement that require correction on the record. The Statement of Reasons for Allowance is not consistent with (at least) the scope of claims 1 and 15. For example, the Statement indicates that "The first bipolar transistor circuit includes a stacked arrangement of transistors, the first control circuit includes an amplifier, stacked arrangement of transistors being coupled to the non-inverting input of the amplifier being coupled to current mirror to provide the current to the current source." Putting aside the grammatical problems with the Examiner's Statement, claim 1 does not require a stacked arrangement of transistors for either the first bipolar transistor circuit or the second bipolar transistor circuit. Expressly, both of those elements are said to have "one or more" transistors. Only in dependent claim 10 is the stacking limitation introduced. There is also no reference in claims 1 or 15 to an amplifier or to anything being coupled to the inverting and non-inverting inputs of the amplifier. Neither do those claims require that the output of the amplifier control the gate of a MOSFET. Accordingly,

Applicant does not believe that any of the claims should be interpreted in light of the Examiner's Statement, which appears to relate more to a disclosed embodiment than to the claimed subject matter.

Respectfully submitted,

By:



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Sir:

REQUEST FOR APPROVAL AND ENTRY OF FORMAL DRAWINGS

Enclosed for filing are five sheets of replacement FORMAL DRAWINGS, Figures 1-6, for the above-referenced patent application.

The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account No. 23/2825.

Respectfully submitted,

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